HARDWARE ACCELERATED SOLUTIONS FOR SEQUENCE ALIGNMENT

ACCELERATING GLOBAL ALIGNMENT WITH GPU-BASED AND FPGA-BASED SOLUTIONS

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ABSTRACT

This thesis presents a GPU-based and FPGA-based implementation of a global sequence alignment algorithm. The proposed approach is based on the Needleman-Wunsch algorithm, which is widely used in bioinformatics for pairwise sequence alignment. Two implementations have been developed using Apple's Metal API for a GPU implementation, and Verilog for an FPGA implementation. The results show that both approaches achieve a notable speedup compared to equivalent non-accelerated implementations.

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ACRONYMS

UMA	Unified Memory Architecture
FPGA	Field Programmable Gate Array
GPU	Graphics Processing Unit
SoC	System-on-Chip
SIMD	Single Instruction/Multiple Data
FGMT	Fine-Grained Multithreading
HDL	Hardware Description Language
CLB	Configurable Logic Block
GCUPS	Giga Cell Updates Per Second
HVL	Hardware Verification Language
PU	Processing Unit

Man only likes to count his troubles;
he doesn't calculate his happiness.

— Fyodor Dostoevsky

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